

**Notice of Allowability**

Application No.

09/880,090

Examiner

Paulos M. Natnael

Applicant(s)

SATO, YASUNORI

Art Unit

2614

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Appeal brief filed 6/20/05.
2. ☒ The allowed claim(s) is/are 1,2,4-7,10-18, renumbered as 1,2,3-6,7-15.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some\* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

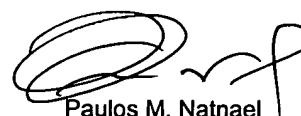
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

  
Paulos M. Natnael  
Primary Examiner  
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## DETAILED ACTION

### *Allowable Subject Matter*

1. Claims 1,2,4-7,10-18 are allowed.
2. The following is an examiner's statement of reasons for allowance: the prior art fails to disclose a control circuit comprising, a counter circuit that counts a pixel number of each line in the input data; and, a judgment circuit that calculates a difference between the standard number and the pixel number counted by the counter circuit, and a selector combining the delayed input data in response to the calculated difference signal to generate as an output data combined input data having the standard number of pixels, as in claim1;

A video signal control circuit receiving a video signal including a plurality of lines each of which nominally includes a standard number of pixels as an input data, the video signal control circuit comprising, memory circuit which the input data can be written in and read from, which includes two one-port memories, wherein the input data are alternately written in the two one-port memories, and the written input data are alternately read from the two one-port memories, an address generation circuit that outputs a write address or a read address to the memory circuit, a counter circuit that counts a pixel number of each line in the input data; a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates a new address value in accordance with an address value generated by the address generation circuit and the calculated difference; an

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output selector combining the input data read from the memory circuit based on the new address to generate as an output data combined input data having the standard number of pixels, as in claim 6; and, a video signal control circuit that processes a video signal of which one line is composed of plural pixels as an input data, comprising: a memory circuit including a two-port memory that is able to write in and read out the input data in parallel; an address generation circuit that outputs a write address or a read address to the memory circuit; a counter circuit that counts a pixel number of each line in the input data; a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates a new address value in accordance with an address value generated by the address generation circuit and a delay on the basis of the calculated difference; wherein the address generation circuit generates the write address signal or the read address signal on the basis of the address value calculated by the judgment circuit, and when there is a difference between the pixel number of the input data read from the memory circuit and that of the input data written in the memory circuit, some of the plural read addresses each corresponding to the plural data to be read are repeated or deleted, in accordance with the difference between the pixel numbers, the input data read from the memory circuit according to the plural read addresses constituting an output data of the video signal control circuit, as in claim 7.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

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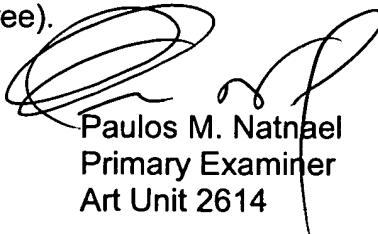
accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (571) 272-7354. The examiner can normally be reached on 10:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571)272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Paulos M. Natnael  
Primary Examiner  
Art Unit 2614

Pmn  
September 6, 2005